

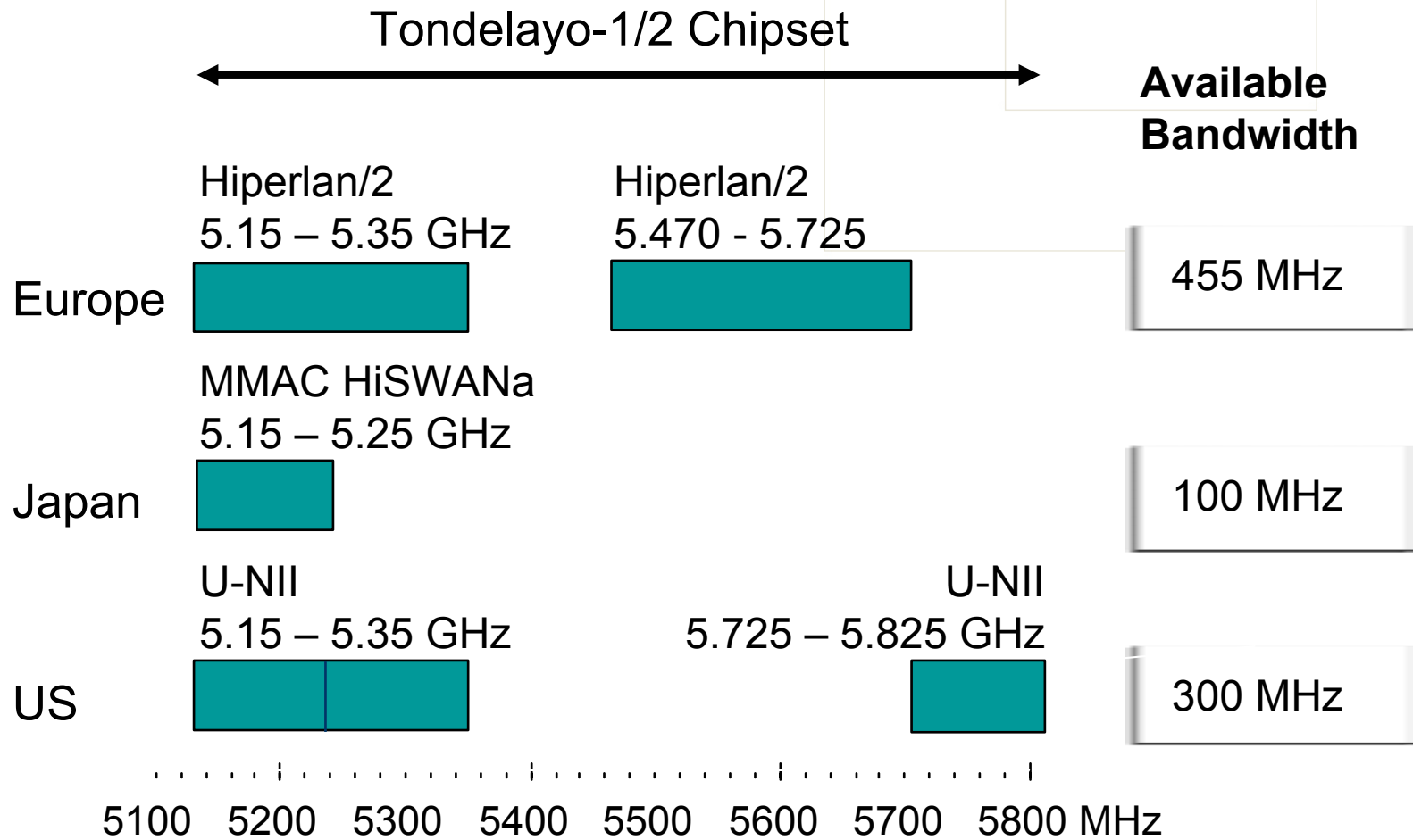
802.11a+b Dual-Mode Architectures

Gerhard Fettweis

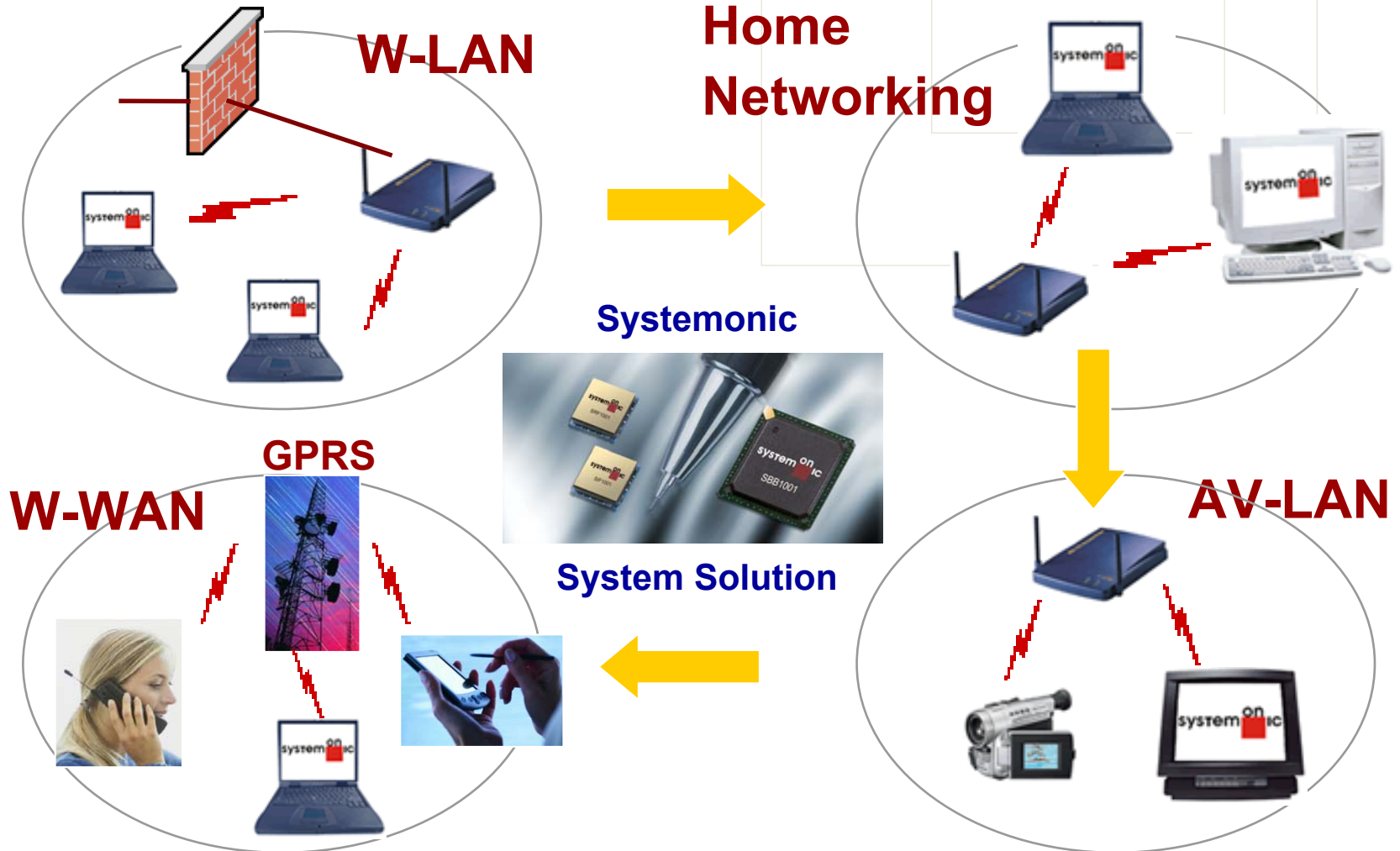
August 29, 2002



World Wide Spectrum Allocation 5 GHz



Target Wireless Market



Waveform Requires Sample Rate = $n \cdot 20\text{MHz}$ for simple implementation

- 64 Samples per 3.2 microsecond period

80 MHz Sample Rate Allows for Simple Digital Downconversion and I/Q Generation

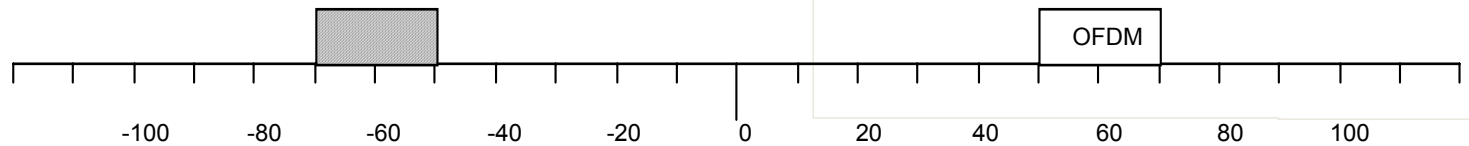
- Complex Wave Digital Polyphase Filter (IIR Filter) implemented
- Can down-convert, decimate and filter in one operation

Normal Choices are 20MHz and 60MHz (Image of -20MHz)

60MHz Selected to simplify analog filtering constraints

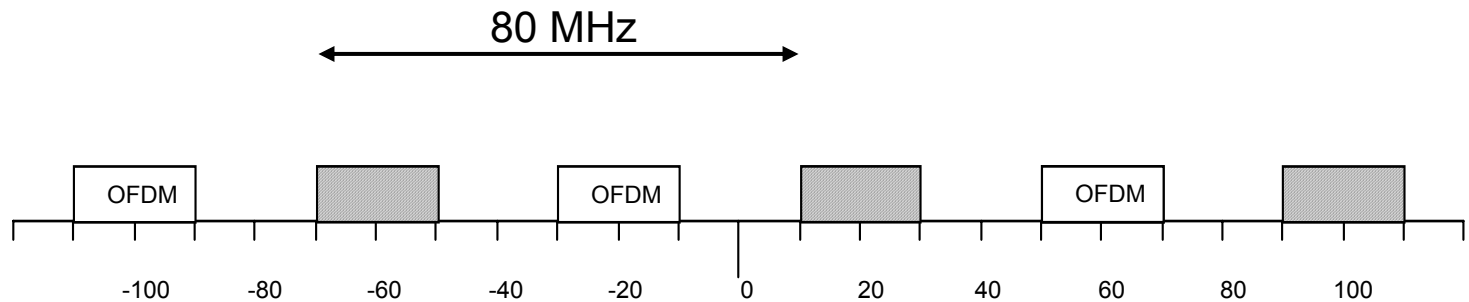
Sampling Frequency Diagram

Spectrum at IF analog Rx output

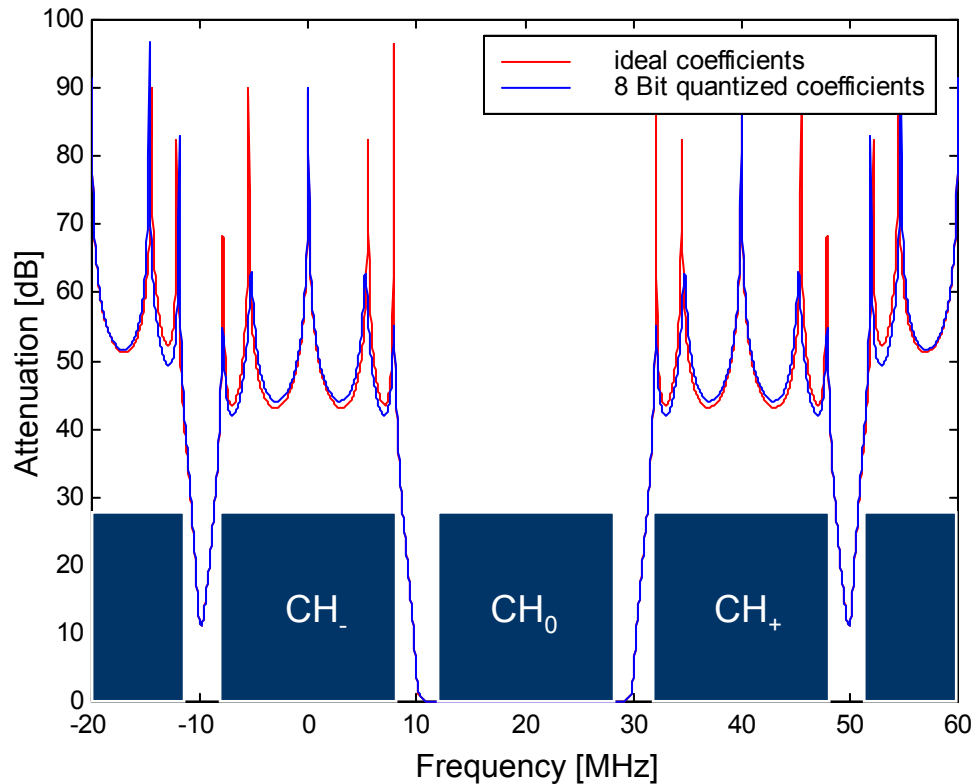


Spectrum of sampled signal

80 MHz sampling



I/Q Filter Performance (Digital I/Q)



Recursive, complex Wave Digital Filter

Adjacent channel suppression >40 dB

IQ image suppression >48 dB

SiGe vs. CMOS – the process question

System Requirements

- Constellation Accuracy is Driven by Phase, Amplitude Error
- Using Real Signals (Not I/Q) Lets Synthesizer Use Majority of Error Budget

Existing Synthesizer

- Off Chip VCO, PLL, Loop Filter Network
- -37.5dBc Integrated Phase Noise (Equivalent to 1.09° of Error)
 - BER (64QAM) = 10^{-5} for a CNR = 25dB

State of the Art CMOS Synthesizer (Paper by Rategh, et. al.)

- Integrated on Chip
- -21.4dBc Integrated Phase Noise (Equivalent to 6.87° of Error)
 - BER (64QAM) = .05 for a CNR = 25dB (PER = 100%)

System Impact and Tradeoffs:

- CMOS VCO's Cause Tremendous Increase in Bit Error Rate (BER) -> less performance
- Off Chip Components Cost More (\$5.65 for Dual PLL and 2 VCO's)
- High Performance VCO's & PLL's Allow Relaxing Other Component Specs

Flicker Noise (1/f Noise) is a Greater Problem for CMOS Devices

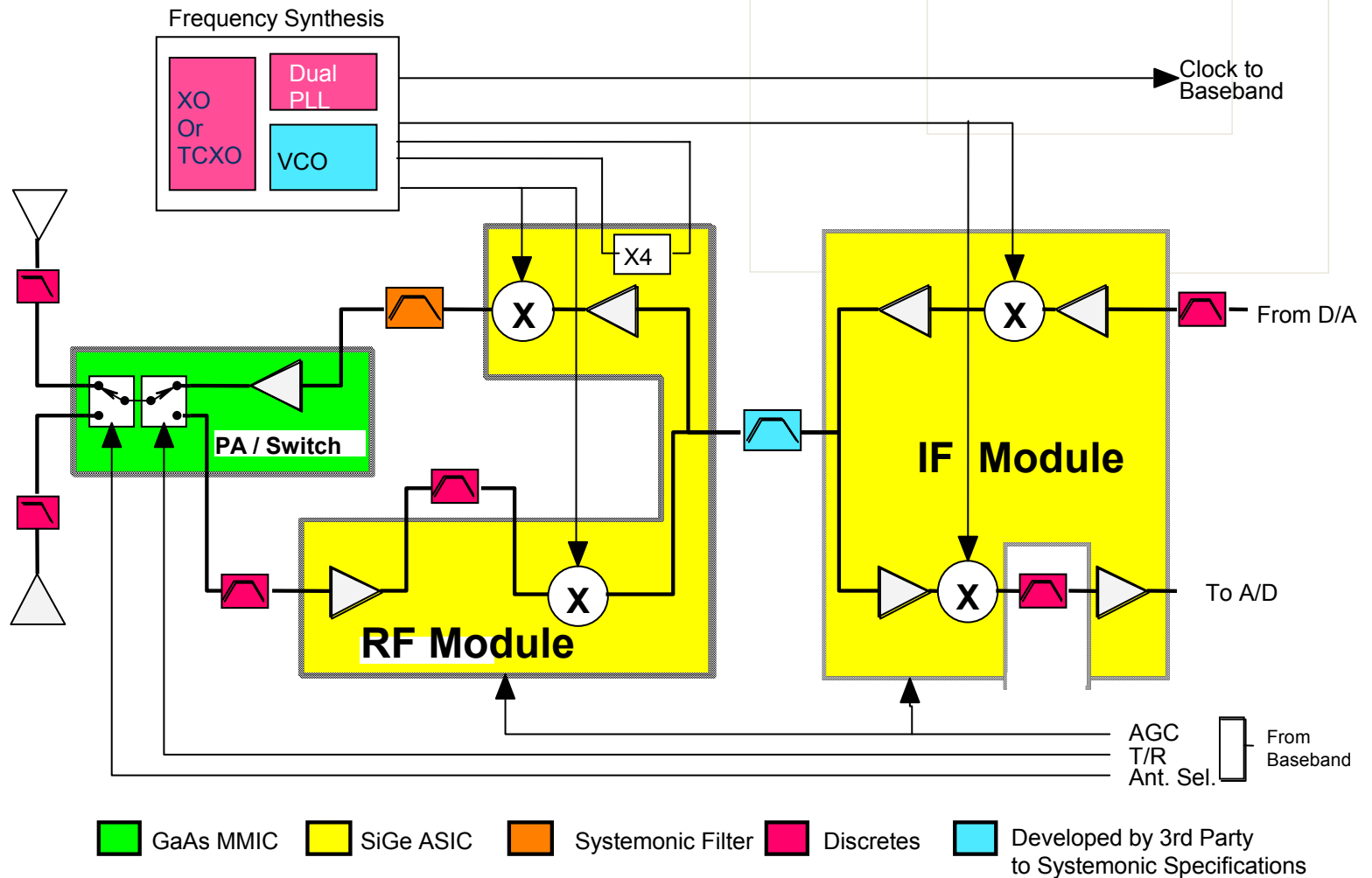
- Tends to be modulated onto the RF signal
- Flicker noise sees high conversion gain in mixers with a baseband output,
- Main way to reduce it in MOS devices is to increase the transistor's size
 - Decreases RF Gain
 - Increased die size and power dissipation

Power Handling and Scaling

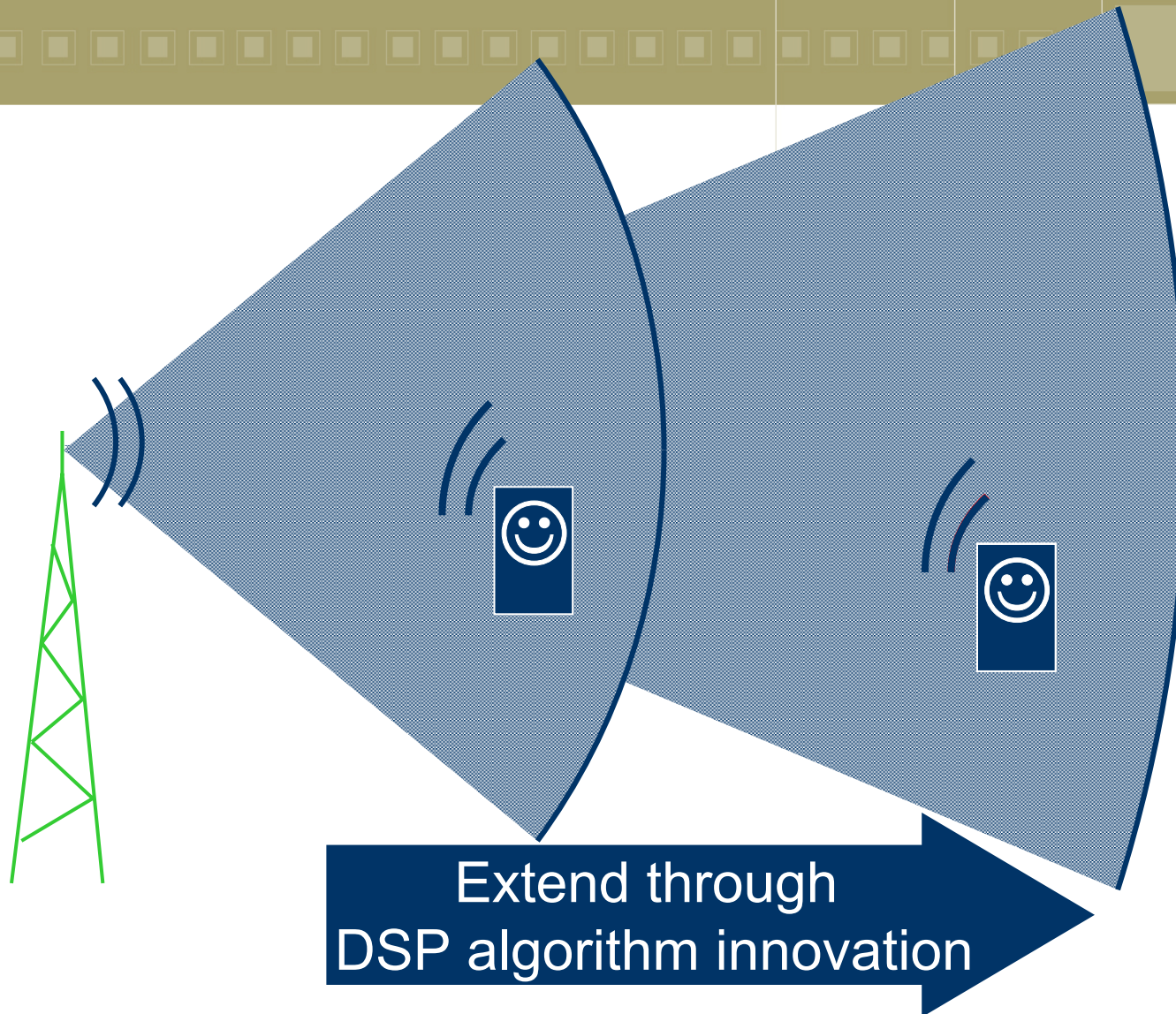
- Analog CMOS devices do not scale with geometry
- SiGe devices' higher f_T requires less gain stages, less power for given P1dB

Tondelayo™ RF & IF Chips Are Fabricated With SiGe

RF Subsystem 802.11a– Technology Mix



The Range/Coverage Limitation



Systemonic's DSP Based Approach

Apply Flexibility (Programmability) Where it is Required

Tailor the Programmable Platform to the Applications Needs

- Processing power (datapath parallelism, SIMD)
- Instruction set architecture (ISA)
- I/O, peripherals and memory subsystem

Design From a Common Architecture Data Base

- Highly automated generation of tailored derivatives
- Generation of SW development tools from same data base

DSP Architecture

- SIMD mode + flexible datapath interface
 - Optimized in conjunction with algorithm design
- SISD mode 32 bit RISC, 16/32 bit DSP
 - allows compiler/programmer friendly programming

DSP vs. Dedicated Hardware

DSP Advantages

- Flexibility
 - DSPs move implementation into software
 - Re-usability of DSPs is higher than dedicated ASICs
- Upgrade capability
 - Evolution of algorithms possible
 - Ability to upgrade, track, and follow standards
- Time to market
 - Parallel validation of hardware and algorithms possible
- Reduction of Design Risk
 - Algorithms are often validated in the field
 - Later algorithm fixes are possible

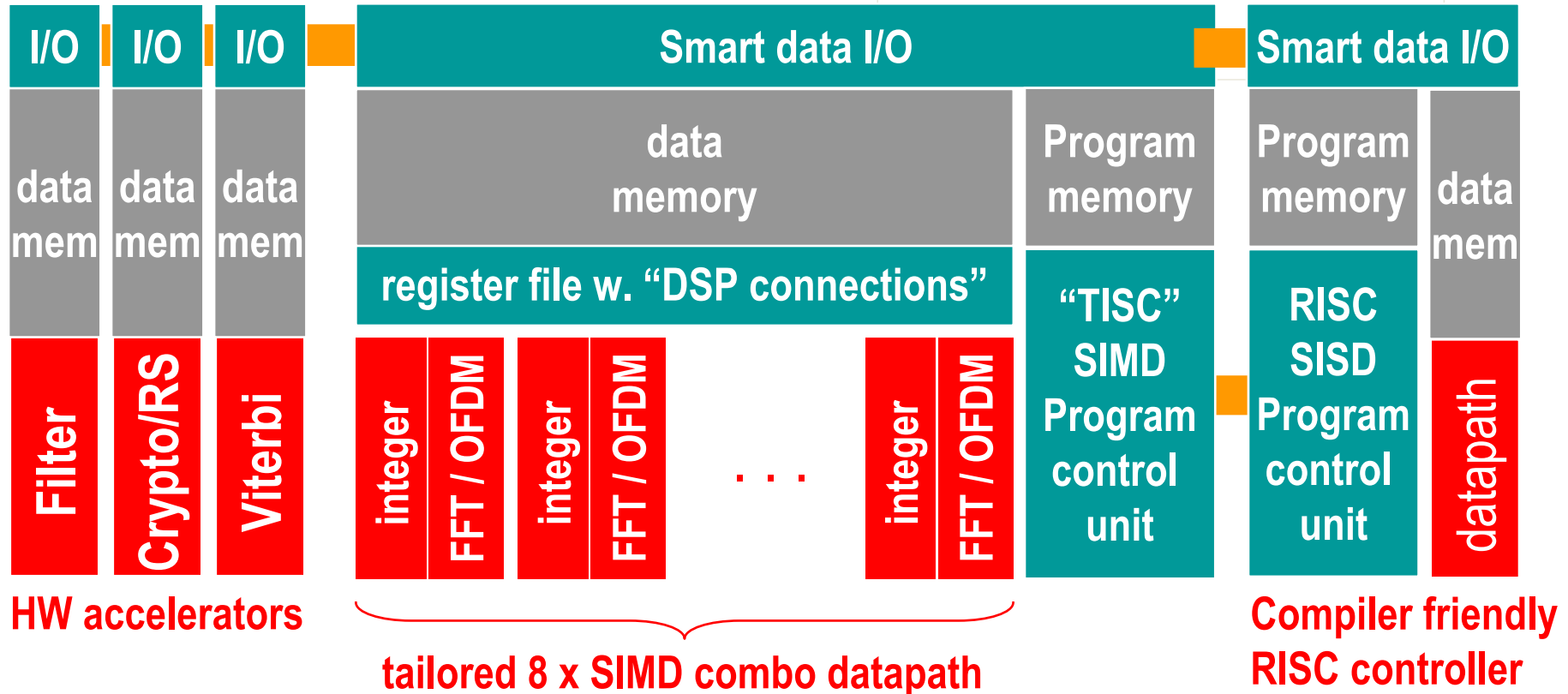
Traditional Hardware Advantages

- More efficient use of real estate (die area) = lower cost
- Lower Power

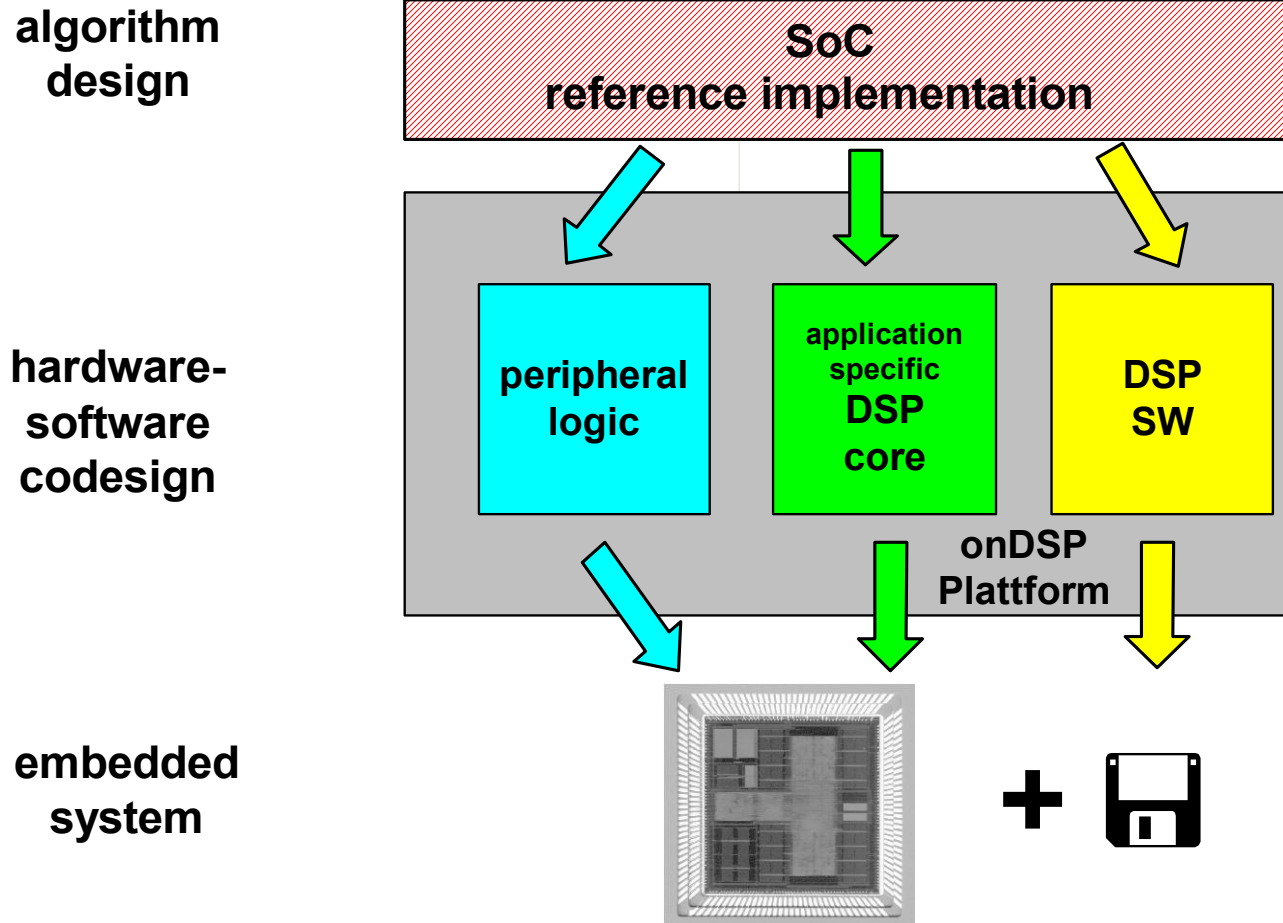
OnDSP: Tailored 802.11 Baseband Solution

ASIC-like tailored solution with software flexibility

- HW elements for fixed application
- FW implementation for wireless performance sensitive elements
- SW implementation for complex control

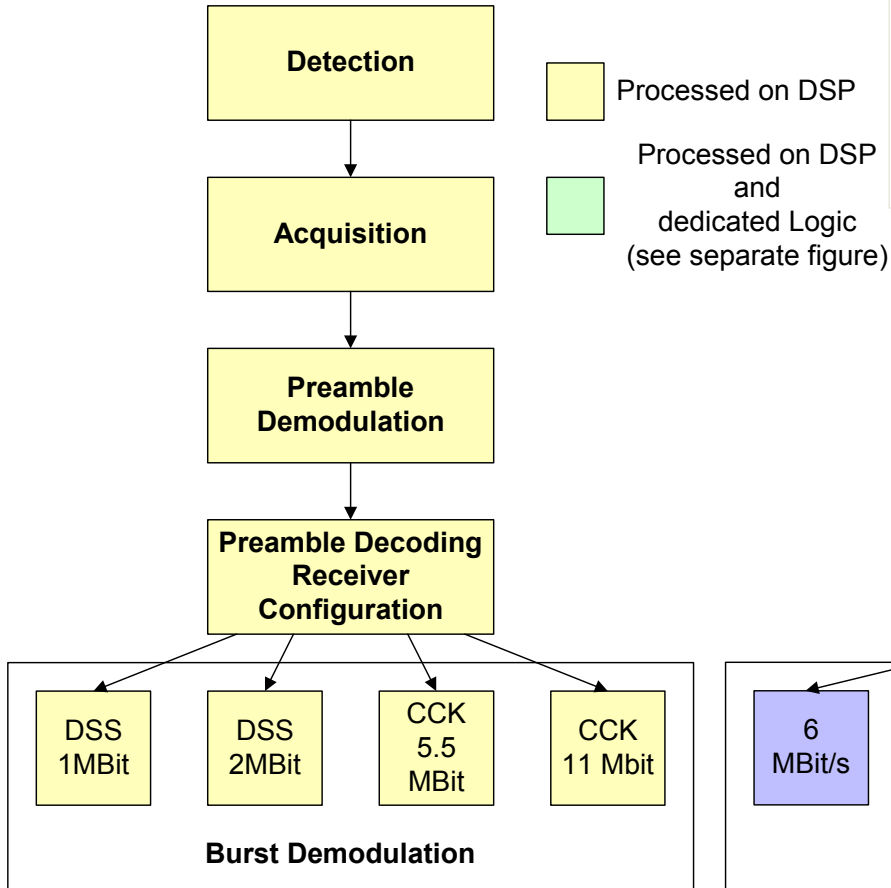


DSP Based Design Process

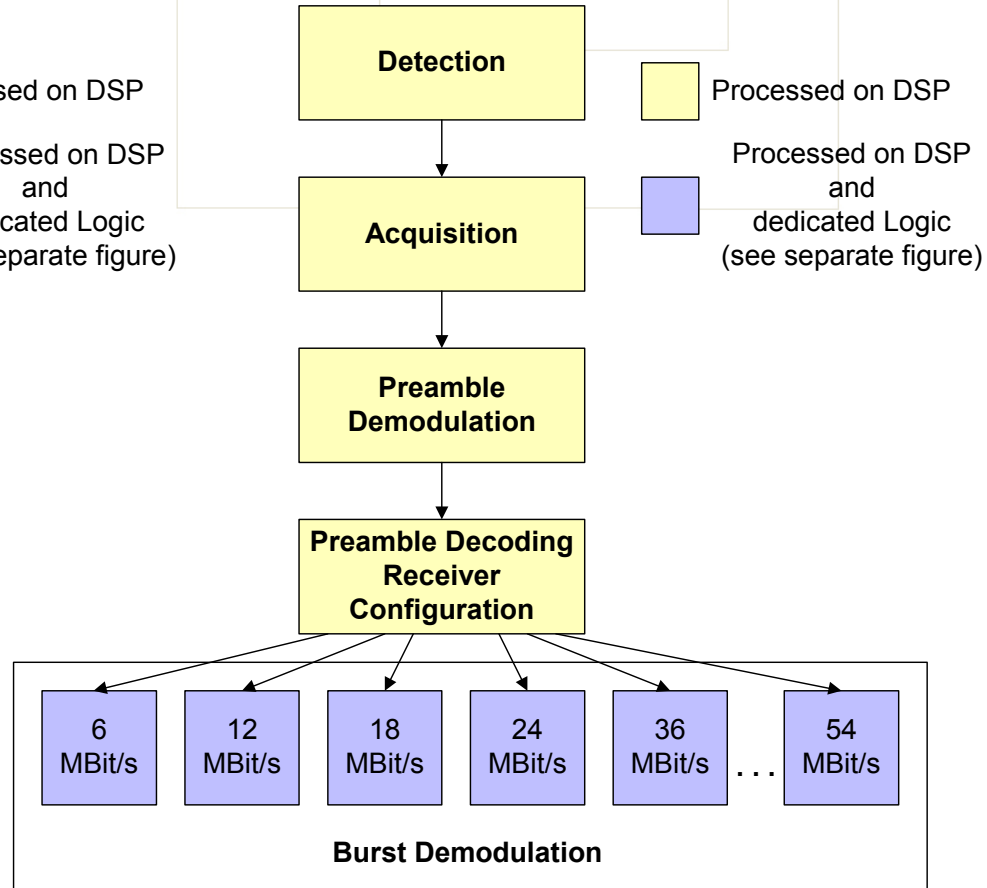


Acquisition Processing

802.11b Signal Acquisition /Preamble Processing



802.11a Signal Acquisition /Preamble Processing



Embedded Processor vs. Host Based MAC

Embedded Processor Advantages

- Single software platform (typically Arm7/9 based)
- Can tightly couple the processor to the modem function
- Not dependant on PCI bus performance

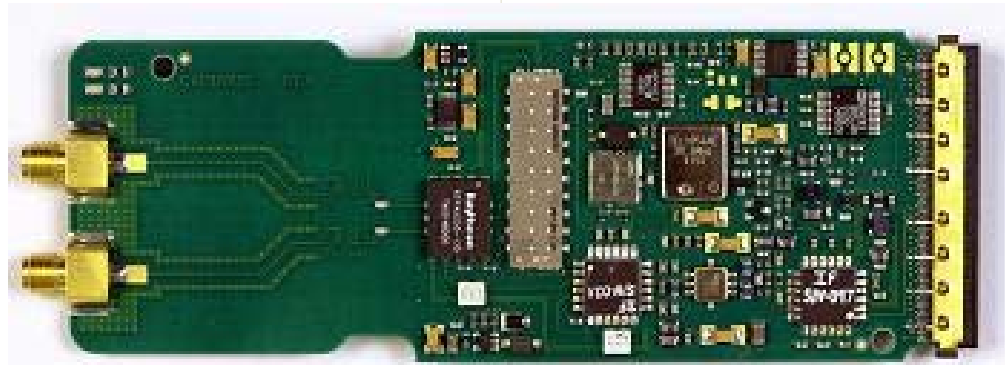
Host Based Processor Advantages

- Reduced die size and power dissipation
- No external flash, SRAM/DRAM required
- Provides more flexibility for access point applications
 - May share processor with access point or other network interface
 - Moves QOS queues off chip to host memory
- Eliminates royalty for embedded processor

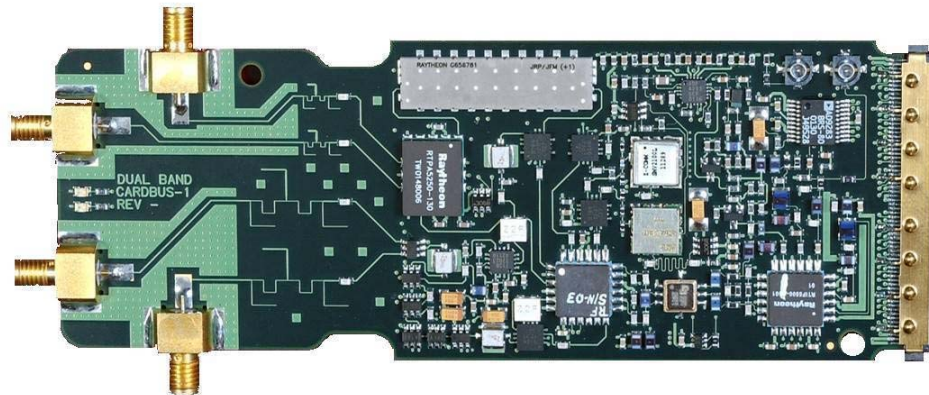
Systemonic Chose Host Based MAC

Systemonic 802.11a and a/b Cardbus NIC

Ref. Design V 0.1
802.11 "a"



Ref. Design V 0.1
802.11 "a+b"



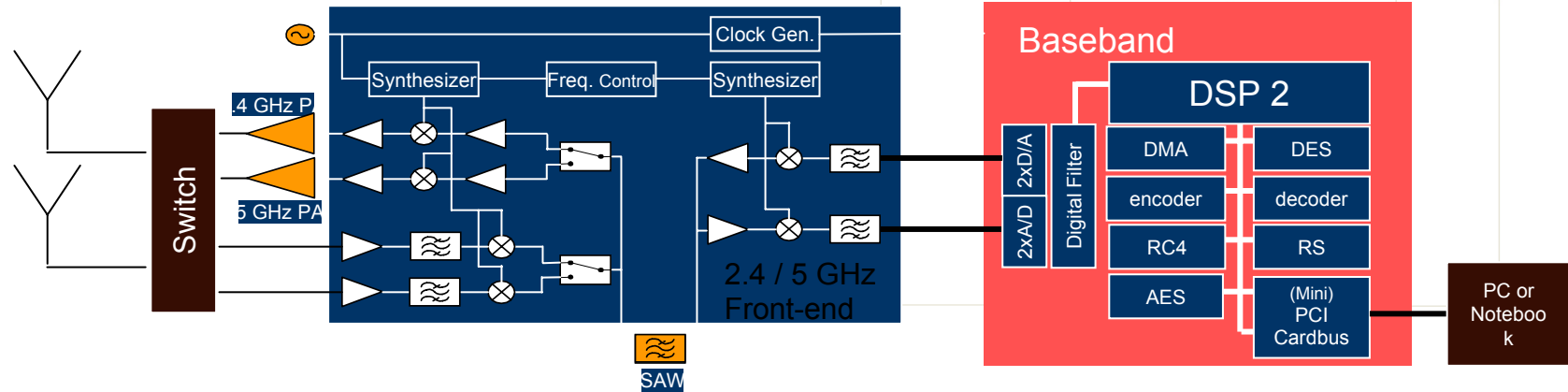
Tondelayo 2

A Complete Solution for IEEE 802.11x

August 29, 2002

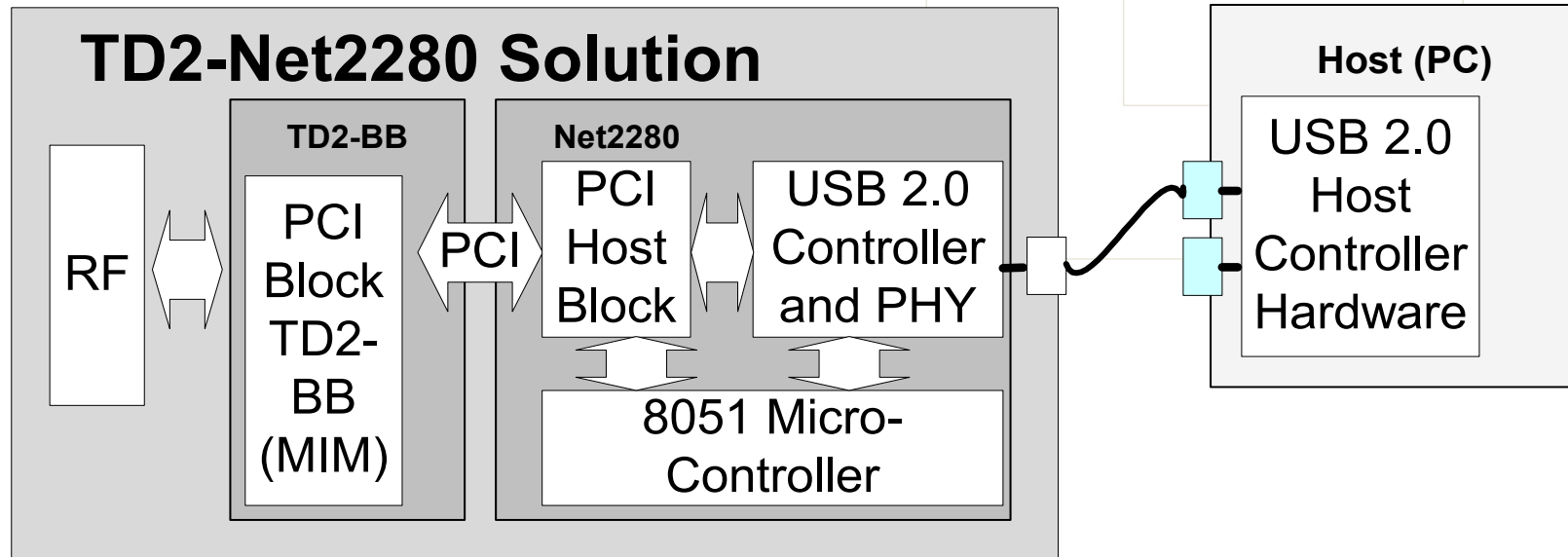


Tondelayo 2 System Solution



Frequency Range	2.400 - 2.500 GHz; 5.170 - 5.330 GHz; 5.490 - 5.815 GHz; 4.910 - 4.990 GHz (/w ext. LO); 5.03 - 5.091 GHz; 5.850 - 5.925 GHz
Concept	Superheterodyne, IF interface to BB
Number of Chips	2 + PA/Switch
Technologies	SiGe RF + 0.18μ CMOS baseband
Data Rates	1, 2, 5.5, 11, 6, 9, 12, 18, 24, 36, 48, 54, 64, 72 Mbps
Range (Line of Sight)	70 m @ 54 Mbps
Antenna Diversity	Yes (switched antenna diversity)
Protocol/Firmware	IEEE 802.11 a, b, g, e, h, i, (HiperLAN/2 possible)
Driver/Operating System	Microsoft Windows 98SE, ME, 2000, XP

TD-2 USB2.0 Solution



- **IEEE 802.11 a/b/g support over USB2.0**
- **IEEE 802.11 h and i optional**

Tondelayo 2 RF Key Parameters

- **Power**
 - Supply voltage 3V
 - Low power consumption
- **PA driver integrated**
- **Synthesizer & VCO fully integrated**
- **Transmit power control for 11h and HiperLAN/2**
- **RSSI provided to baseband processor**
- **80 MHz clock output for baseband processor (integrated XO with external quartz)**
- **Noise figure: 3 dB**

Performance – Range

SiGe RF gives Systemonic an Edge

Technology plays an important role in defining the range

- CMOS is not able to compete with SiGe today
- SiGe receive chain allows better sensitivity – hence range

Systemonic has calculated substantial range (70m) in line of sight conditions (without a high gain antenna) is possible

- Under typical office environment (1 or 2 walls/partitions), calculations show we can achieve 30+ meters

	Range	Data Rate
Magis (11a)	75m	40Mbps
Atheros (11a)	<30m	54Mbps
Tondelayo 2 (11a)	70m	54Mbps

Tondelayo – Systemonic's First Product Line

Complete Wireless LAN Solution

Multi-mode RF Front-end

- 2.4 - 2.5 GHz
- 5 - 6 GHz

Multi-protocol Baseband-to-Driver

- 802.11a & b
- Additional support for 802.11 e, g, h, i and others as released

PCI, CardBus, PCCard, MAC Software